MT7615 802.11ac Wi-Fi 4x4 Dual-band Single Chip

Version: 0.33
Release date: 2015-10-29

Document Revision History

Revision	Date	Author	Description
0.1	2014-12-23	YW Lin	Initial draft
0.2	2014-12-26	YW Lin	
0.21	2015-01-02	Ben Lin	Updated features and pin layout
0.3	2015-08-18	CH Hung	Update Performance & Current consumption
0.31	2015-08-21	CH Hung	Update feature and pin layout
0.33	2015-10-29	CH Hung	Update DVDD11 range to TBD

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Lists of Tables and Figures

1 System Overview

1.1 General Descriptions

MT7615 is a highly integrated Wi-Fi single chip which supports 1733 Mbps PHY rate. It fully complies with IEEE 802.11ac and IEEE 802.11 a/b/g/n standards, offering feature-rich wireless connectivity at high standards, and delivering reliable, cost-effective throughput from an extended distance.

Optimized RF architecture and baseband algorithms provide superb performance and low power consumption. Intelligent MAC design deploys a high efficient offload engine and hardware data processing accelerators which completely offloads Wi-Fi task of the host processor. MT7615 is designed to support standard based features in the areas of security, quality of service and international regulations, giving end users the greatest performance any time and in any circumstance.

MT7615 supports concurrent dual-band operation at 5GHz and 2.4GHz band (DBDC, Dual-Band-Dual-Concurrent). It enables diversified applications that require one link at 2.4GHz band, and the other at less crowded 5GHz band simultaneously.

With the advent of 802.11ac, multiuser MIMO (MU-MIMO) is defined. MT7615 supports MU-MIMO with different configurations. An AP is able to use its antenna arrays to transmit multiple frames to different clients at the same time and over the same frequency spectrum.

1.2 Features

- Supports 4x4 4SS 11ac wave2 MU-MIMO and 160MHz channels
- MU-MIMO configurations of
  - 4 users: 4*1ss
  - 3 users: 2*1ss + 1*2ss or 3*1ss
  - 2 users: 2*2ss or 1*1ss + 1*2ss or 2*1ss
- Supports 5, 10, 20, 40, 80, 80+80, and 160MHz channels
- Embedded ARM Cortex R4 processor for full host CPU offload
- Embedded 32-bit RISC microprocessor
- iNIC Gen2 with full Wi-Fi offload
- Highly integrated RF with 40nm low power process
- 4T4R with support of up to 1733Mbps PHY rate
- Configurable 4x4/3x3 or 2x2n+2x2ac DBDC
- Noise mitigation:
  - Supports background scan function for fast channel switching
  - Supports spectrum analysis for non-Wi-Fi signals
- Intelligent power saving
- Hardware-based Airtime Fairness (QoS)
- Integrate high efficiency internal 2.4G/5G PAs

- Intelligent Calibration (iCal) reduces the production time
- Supports external PA/LNA/TRSW design
- Proprietary LTE coexistence over UART
- WoWLAN via GPIO (client mode), supports Host Sleep (AP mode)
- Compact 12mm*12mm DRQFN118 package with PCIe Gen2 interface

1.3 Operation Systems Support

- Linux
- OpenWrt
- Android

1.4 Block Diagram

Figure 1-1. MT7615 block diagram

2 Product Descriptions

2.1 Pin Layout

MT7615 uses a 118 pins DR-QFN package. The pin order is shown below.

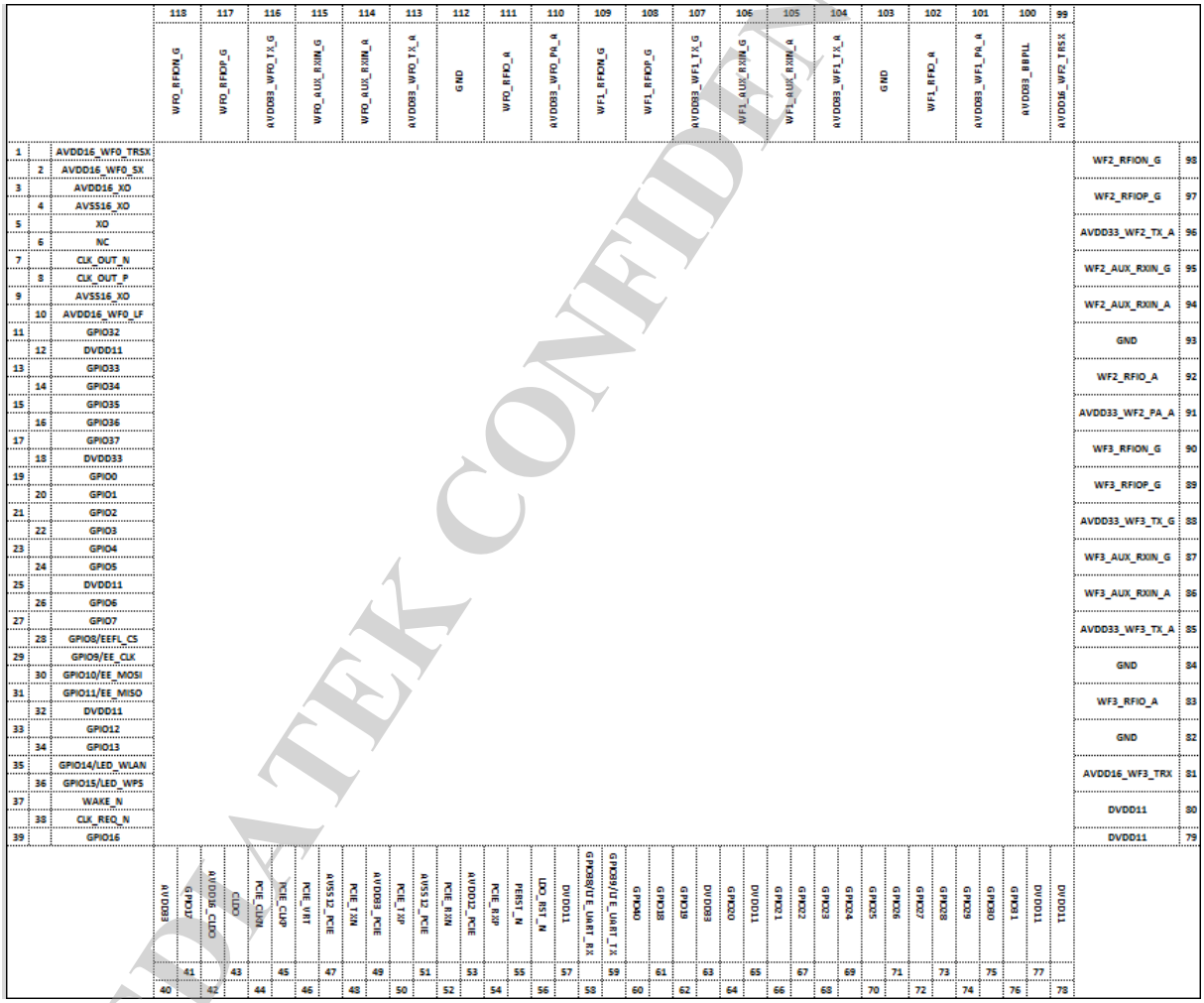


Figure 2-1. Top view of MT7615 DRQFN pin-out

2.2 PIN Description

Table 2-1. Pin descriptions

DRQFN 118	Pin name	Pin description	Default PU/PD	I/O	Supply domain

DRQFN 118	Pin name	Pin description	Default PU/PD	I/O	Supply domain
Reset and clocks					
56	LDO_RST_N	External system reset active low	PU	Input	DVDD33
5	XO	Crystal input or external clock input	N/A	Input	AVDD16_XO
PCIe interface					
37	WAKE_N	Request system to wake from the sleep/suspend state	PU	In/out	DVDD33
38	CLK_REQ_N	Reference clock request signal	PD	In/out	DVDD33
55	PERST_N	PCIe functional reset	PU	Input	DVDD33
44	PCIE_CLKN	PCIe differential reference clock	N/A	Input	AVDD33_PCIE
45	PCIE_CLKP	PCIe differential reference clock	N/A	Input	AVDD33_PCIE
48	PCIE_TXN	PCIe transmit differential pair	N/A	Output	AVDD33_PCIE
50	PCIE_TXP	PCIe transmit differential pair	N/A	Output	AVDD33_PCIE
52	PCIE_RXN	PCIe receive differential pair	N/A	Input	AVDD33_PCIE
54	PCIE_RXP	PCIe receive differential pair	N/A	Input	AVDD33_PCIE
46	PCIE_VRT	PCIe resister reference	N/A	Analog	
EEPROM/flash interface					
28	GPIO8/EEFL_CS	External chip select	PD	In/out	DVDD33
29	GPIO9/EE_CLK	External clock	PD	In/out	DVDD33
30	GPIO10/EE_MOSI	External memory data output	PD	In/out	DVDD33
31	GPIO11EE_MISO	External memory data input	PD	In/out	DVDD33
Programmable I/O					
11	GPIO32	Programmable input/output	PD	In/out	DVDD33
13	GPIO33	Programmable input/output	PD	In/out	DVDD33
14	GPIO34	Programmable input/output	PD	In/out	DVDD33
15	GPIO35	Programmable input/output	PD	In/out	DVDD33
16	GPIO36	Programmable input/output	PD	In/out	DVDD33
17	GPIO37	Programmable input/output	PD	In/out	DVDD33
19	GPIO0	Programmable input/output	PD	In/out	DVDD33
20	GPIO1	Programmable input/output	PD	In/out	DVDD33
21	GPIO2	Programmable input/output	PD	In/out	DVDD33
22	GPIO3	Programmable input/output	PD	In/out	DVDD33
23	GPIO4	Programmable input/output	PD	In/out	DVDD33
24	GPIO5	Programmable input/output	PD	In/out	DVDD33
26	GPIO6	Programmable input/output	PD	In/out	DVDD33
27	GPIO7	Programmable input/output	PD	In/out	DVDD33
28	GPIO8	Programmable input/output	PD	In/out	DVDD33
29	GPIO9	Programmable input/output	PD	In/out	DVDD33
30	GPIO10	Programmable input/output	PD	In/out	DVDD33
31	GPIO11	Programmable input/output	PD	In/out	DVDD33
33	GPIO12	Programmable input/output	PD	In/out	DVDD33
34	GPIO13	Programmable input/output	PD	In/out	DVDD33

DRQFN 118	Pin name	Pin description	Default PU/PD	I/O	Supply domain
39	GPIO16	Programmable input/output	PU	In/out	DVDD33
41	GPIO17	Programmable input/output	PU	In/out	DVDD33
61	GPIO18	Programmable input/output	PU	In/out	DVDD33
62	GPIO19	Programmable input/output	PU	In/out	DVDD33
64	GPIO20	Programmable input/output	PU	In/out	DVDD33
66	GPIO21	Programmable input/output	PD	In/out	DVDD33
67	GPIO22	Programmable input/output	PD	In/out	DVDD33
68	GPIO23	Programmable input/output	PD	In/out	DVDD33
69	GPIO24	Programmable input/output	PU	In/out	DVDD33
70	GPIO25	Programmable input/output	PU	In/out	DVDD33
71	GPIO26	Programmable input/output	PU	In/out	DVDD33
72	GPIO27	Programmable input/output	PU	In/out	DVDD33
73	GPIO28	Programmable input/output	PU	In/out	DVDD33
74	GPIO29	Programmable input/output	PD	In/out	DVDD33
75	GPIO30	Programmable input/output	PD	In/out	DVDD33
76	GPIO31	Programmable input/output	PD	In/out	DVDD33
60	GPIO40	Programmable input/output	PD	In/out	DVDD33
LED					
35	GPIO14/LED_WLAN	Programmable open-drain LED controller	PU	In/out	DVDD33
36	GPIO15/LED_WPS	Programmable LED controller	PU	In/out	DVDD33
WIFI radio interface					
83	WF3_RFIO_A	WF3 RF a-band RF port	N/A	In/Out	
86	WF3_AUX_RXIN_A	WF3 RF a-band auxiliary RF LNA port	N/A	Input	
87	WF3_AUX_RXIN_G	WF3 RF g-band auxiliary RF LNA port	N/A	Input	
89	WF3_RFIOP_G	WF3 RF g-band RF port	N/A	In/Out	
90	WF3_RFION_G	WF3 RF g-band RF port	N/A	In/Out	
92	WF2_RFIO_A	WF2 RF a-band RF port	N/A	In/Out	
94	WF2_AUX_RXIN_A	WF2 RF a-band auxiliary RF LNA port	N/A	Input	
95	WF2_AUX_RXIN_G	WF2 RF g-band auxiliary RF LNA port	N/A	Input	
97	WF2_RFIOP_G	WF2 RF g-band RF port	N/A	In/Out	
98	WF2_RFION_G	WF2 RF g-band RF port	N/A	In/Out	
102	WF1_RFIO_A	WF1 RF a-band RF port	N/A	In/Out	
105	WF1_AUX_RXIN_A	WF1 RF a-band auxiliary RF LNA port	N/A	Input	
106	WF1_AUX_RXIN_G	WF1 RF g-band auxiliary RF LNA port	N/A	Input	
108	WF1_RFIOP_G	WF1 RF g-band RF port	N/A	In/Out	
109	WF1_RFION_G	WF1 RF g-band RF port	N/A	In/Out	
111	WF0_RFIO_A	WF0 RF a-band RF port	N/A	In/Out	
114	WF0_AUX_RXIN_A	WF0 RF a-band auxiliary RF LNA port	N/A	Input	
115	WF0_AUX_RXIN_G	WF0 RF g-band auxiliary RF LNA port	N/A	Input	
117	WF0_RFIOP_G	WF0 RF g-band RF port	N/A	In/Out	

DRQFN 118	Pin name	Pin description	Default PU/PD	I/O	Supply domain
118	WF0_RFION_G	WF0 RF g-band RF port	N/A	In/Out	
7	CLK_OUT_N	XTAL buffered clock output	N/A	Output	
8	CLK_OUT_P	XTAL buffered clock output	N/A	Output	
PMU					
43	CLDO	LDO 1.15V output	N/A	Output	
42	AVDD16_CLDO	Digital LDO 1.68V power supply	N/A	Power	
40	AVDD33	3.3V power supply	N/A	Power	
LTE coexistence					
58	GPIO38/LTE_UART_RX	UART RX	PU	In/out	DVDD33
59	GPIO39/LTE_UART_TX	UART TX	PU	In/out	DVDD33
Power supplies					
18, 63	DVDD33	Digital 3.3v I/O power supply	N/A	Power	
12, 25, 32,57,65 ,77,78,7 9, 80	DVDD11	Digital 1.15v core power supply	N/A	Power	
49	AVDD33_PCIE	PCIe 3.3V power supply	N/A	Power	
53	AVDD12_PCIE	PCIe 1.2V power supply	N/A	Power	
85	AVDD33_WF3_TX_A	RF 3.3v power supply	N/A	Power	
88	AVDD33_WF3_TX_G	RF 3.3v power supply	N/A	Power	
91	AVDD33_WF2_PA_A	RF 3.3v power supply	N/A	Power	
96	AVDD33_WF2_TX_A	RF 3.3v power supply	N/A	Power	
99	AVDD16_WF2_TRSX	RF1.68v power supply	N/A	Power	
100	AVDD33_BBPLL	BBPLL 3.3v power supply	N/A	Power	
101	AVDD33_WF1_PA_A	RF 3.3v power supply	N/A	Power	
104	AVDD33_WF1_TX_A	RF 3.3v power supply	N/A	Power	
107	AVDD33_WF1_TX_G	RF 3.3v power supply	N/A	Power	
110	AVDD33_WF0_PA_A	RF 3.3v power supply	N/A	Power	
113	AVDD33_WF0_TX_A	RF 3.3v power supply	N/A	Power	
116	AVDD33_WF0_TX_G	RF 3.3v power supply	N/A	Power	
81	AVDD16_WF3_TRX	RF 1.68v power supply	N/A	Power	
1	AVDD16_WF0_TRSX	RF 1.68v power supply	N/A	Power	
2	AVDD16_WF0_SX	RF 1.68v power supply	N/A	Powers	
3	AVDD16_XO	XTAL 1.68v power supply	N/A	Power	
10	AVDD16_WF0_LF	RF 1.68v power supply	N/A	Power	
47,51	AVSS12_PCIE	PCIe ground	N/A	Ground	
4,9	AVSS16_XO	XTAL ground	N/A	Ground	
82,84,9 3,103,11 2	GND	RF ground	N/A	Ground	

DRQFN 118	Pin name	Pin description	Default PU/PD	I/O	Supply domain
6	NC	Reserved	N/A	N/A	
E-PAD	VSS	Ground	N/A	Ground	

2.3 Strapping Option

Four pins are used to set up the default status of the chip for different normal mode applications. The pins are all internally pulled down. Users can connect the pin with an external small resistor (1KΩ or less) to VDD33 when they want to change the application. Those pins are sampled at Power-On-reset to determine the default status.

GPIO7 is used to identify if the external EEPROM or the internal Efuse is used. GPIO10 is used for testing purpose, and the user should set up normal mode for normal application.

Table 2-2. Strapping option

Name	Usage	Definition	Power down Pull setting(1)	Default strap pull setting(2)	Normal mode pull setting(3)
GPIO6	co-clock input source selection	0: use xtal clock as co-clock input 1: use external clock as co-clock input	High-Z	Pull Down, 75K ohm	Pull Down, 75K ohm (PU/PD adjustable)
GPIO7	EEPROM selection	0: EFUSE 1: EEPROM	High-Z	Pull Down, 75K ohm	Pull Down, 75K ohm (PU/PD adjustable)
GPIO8	co-clock mode selection	0: current mode 1: voltage mode (co-clock output buffer is default turned on)	High-Z	Pull Down, 75K ohm	Pull Down, 75K ohm (PU/PD adjustable)
GPIO10	test mode selection	0: normal mode 1: test mode	High-Z	Pull Down, 75K ohm	Pull Down, 75K ohm (PU/PD adjustable)

Note :
1) PAD pull-up/pull down setting when I/O 3.3V power is not ready.
2) PAD pull-up/pull down setting in strapping mode, i.e. power on reset is asserted or LDO_RST_N is LOW.
3) PAD pull-up/pull down setting in normal mode, i.e. power on reset is de-asserted and LDO_RST_N is HIGH.

2.4 IO Control Option

MT7615 provides 41 configurable I/O functions to support diversified applications. The IO functions can be configured through the control register PINMUX_SEL. It supports external front-end module on dual bands for high power requirement. Open drained IOs are available for WLAN LED. The most common configuration is listed in the table below.

Table 2-3. IO control option

	PAD Name	Function 0	Function 1	Function 2
11	PAD_GPIO32	gpio[32] (I/O)	antsel_0[19] (O)	
12	PAD_GPIO33	gpio[33] (I/O)	antsel_0[18] (O)	
13	PAD_GPIO34	gpio[34] (I/O)	antsel_0[17] (O)	
14	PAD_GPIO35	gpio[35] (I/O)	antsel_0[16] (O)	
16	PAD_GPIO36	gpio[36] (I/O)	antsel_0[15] (O)	
17	PAD_GPIO37	gpio[37] (I/O)	antsel_0[14] (O)	
19	PAD_GPIO0	gpio[0] (I/O)	antsel_0[13] (O)	
20	PAD_GPIO1	gpio[1] (I/O)	antsel_0[12] (O)	
21	PAD_GPIO2	gpio[2] (I/O)	antsel_0[11] (O)	
22	PAD_GPIO3	gpio[3] (I/O)	antsel_0[10] (O)	
23	PAD_GPIO4	gpio[4] (I/O)	antsel_0[9] (O)	n9_debug_uart_tx (O)
24	PAD_GPIO5	gpio[5] (I/O)	antsel_0[8] (O)	cr4_debug_uart_tx (O)
26	PAD_GPIO6	gpio[6] (I/O)	antsel_0[7] (O)	
27	PAD_GPIO7	gpio[7] (I/O)	antsel_0[6] (O)	
28	PAD_GPIO8	gpio[8] (I/O)	antsel_0[5] (O)	
29	PAD_GPIO9	gpio[9] (I/O)	antsel_0[4] (O)	
30	PAD_GPIO10	gpio[10] (I/O)	antsel_0[3] (O)	
31	PAD_GPIO11	gpio[11] (I/O)	antsel_0[2] (O)	
33	PAD_GPIO12	gpio[12] (I/O)	antsel_0[1] (O)	
34	PAD_GPIO13	gpio[13] (I/O)	antsel_0[0] (O)	rbist_ck (I)
35	PAD_GPIO14	led_wlan_od (I/O)		gpio[14] (I/O)
36	PAD_GPIO15	led_wps (O)		gpio[15] (I/O)
39	PAD_GPIO16	eint_in[0] (I)		gpio[16] (I/O)
41	PAD_GPIO17	eint_in[1] (I)		gpio[17] (I/O)
58	PAD_GPIO38	lte_uart_rx (I)		gpio[38] (I/O)
59	PAD_GPIO39	lte_uart_tx (O)	eint_in[2] (I)	gpio[39] (I/O)
60	PAD_GPIO40	gpio[40] (I/O)	eint_in[3] (I)	
61	PAD_GPIO18	n9_debug_uart_tx (O)	antsel_1[13] (O)	gpio[18] (I/O)
62	PAD_GPIO19	mcu_jtms (I)	antsel_1[12] (O)	gpio[19] (I/O)
64	PAD_GPIO20	mcu_jtrst_b (I)	antsel_1[11] (O)	gpio[20] (I/O)
66	PAD_GPIO21	mcu_jtck (I)	antsel_1[10] (O)	gpio[21] (I/O)
67	PAD_GPIO22	mcu_jtdi (I)	antsel_1[9] (O)	gpio[22] (I/O)
68	PAD_GPIO23	mcu_jtdo (O)	antsel_1[8] (O)	gpio[23] (I/O)
69	PAD_GPIO24	mcu_dbgin (I)	antsel_1[7] (O)	gpio[24] (I/O)
70	PAD_GPIO25	mcu_dbgackn (O)	antsel_1[6] (O)	gpio[25] (I/O)
72	PAD_GPIO26	cr4_debug_uart_tx (O)	antsel_1[5] (O)	gpio[26] (I/O)
74	PAD_GPIO27	cr4_jtms (I/O)	antsel_1[4] (O)	gpio[27] (I/O)
76	PAD_GPIO28	cr4_jtrst_b (I)	antsel_1[3] (O)	gpio[28] (I/O)
77	PAD_GPIO29	cr4_jtck (I)	antsel_1[2] (O)	gpio[29] (I/O)
78	PAD_GPIO30	cr4_jtdi (I)	antsel_1[1] (O)	gpio[30] (I/O)
79	PAD_GPIO31	cr4_jtdo (O)	antsel_1[0] (O)	gpio[31] (I/O)

2.5 Package Information

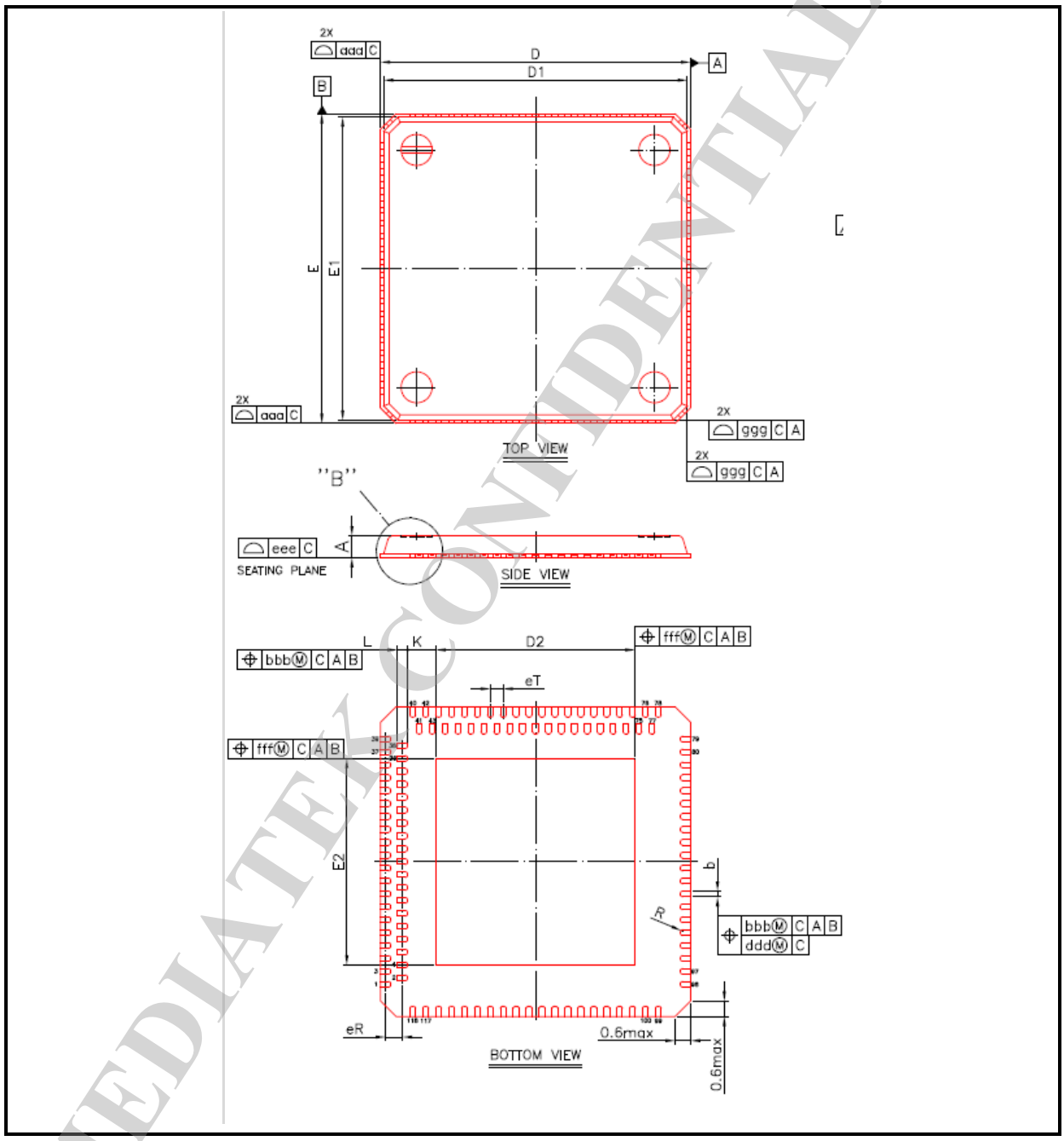
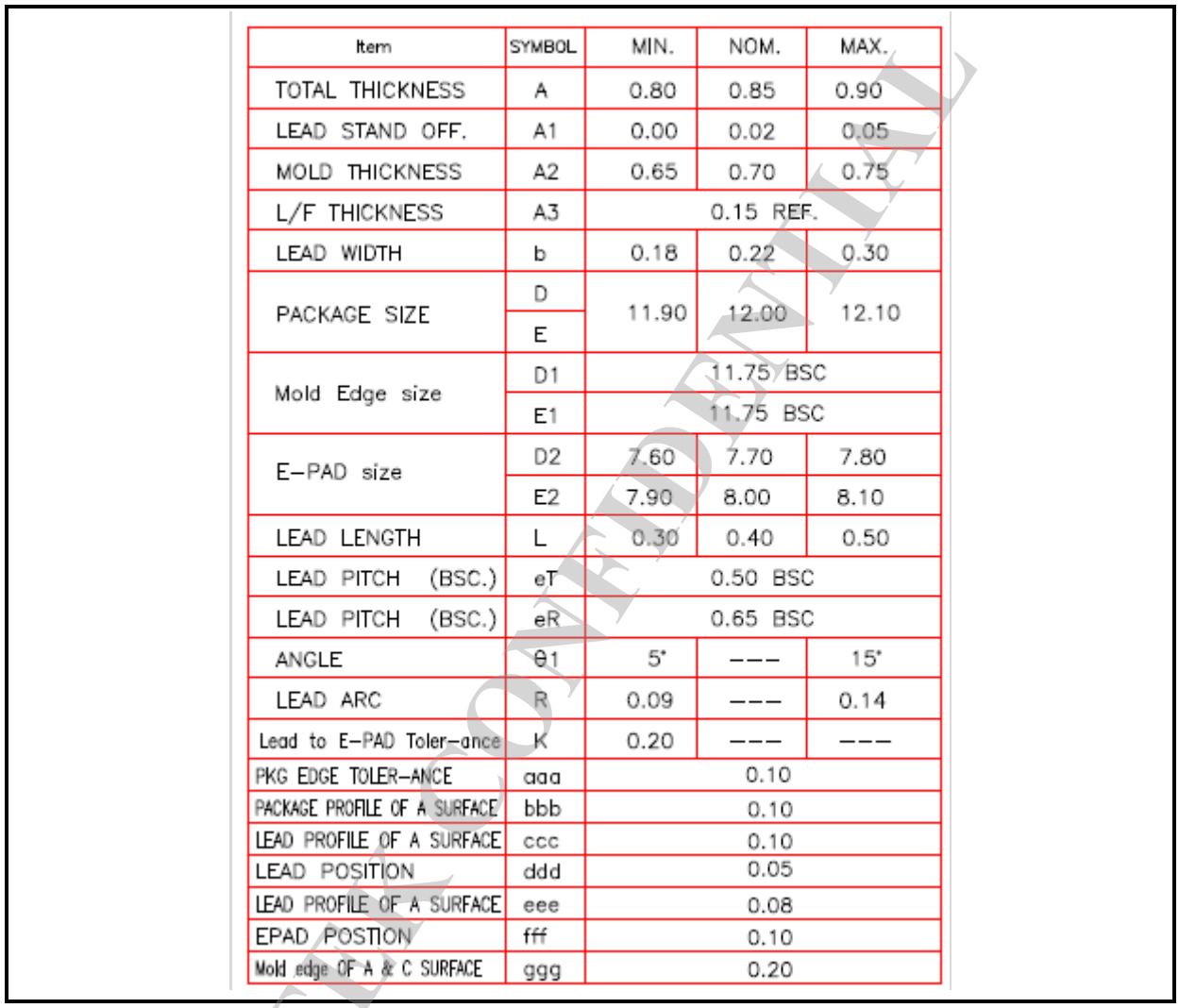


Figure 2-2. Package outline drawing



Item	SYMBOL	MIN.	NOM.	MAX.
TOTAL THICKNESS	A	0.80	0.85	0.90
LEAD STAND OFF.	A1	0.00	0.02	0.05
MOLD THICKNESS	A2	0.65	0.70	0.75
L/F THICKNESS	A3		0.15 REF.	
LEAD WIDTH	b	0.18	0.22	0.30
PACKAGE SIZE	D	11.90	12.00	12.10
	E			
Mold Edge size	D1		11.75 BSC	
	E1		11.75 BSC	
E-PAD size	D2	7.60	7.70	7.80
	E2	7.90	8.00	8.10
LEAD LENGTH	L	0.30	0.40	0.50
LEAD PITCH (BSC.)	eT		0.50 BSC	
LEAD PITCH (BSC.)	eR		0.65 BSC	
ANGLE	θ1	5°	---	15°
LEAD ARC	R	0.09	---	0.14
Lead to E-PAD Toler-ance	K	0.20	---	---
PKG EDGE TOLER-ANCE	aaa		0.10	
PACKAGE PROFILE OF A SURFACE	bbb		0.10	
LEAD PROFILE OF A SURFACE	ccc		0.10	
LEAD POSITION	ddd		0.05	
LEAD PROFILE OF A SURFACE	eee		0.08	
EPAD POSTION	fff		0.10	
Mold edge OF A & C SURFACE	ggg		0.20	

Figure 2-3. Package outline drawing parameters

2.6 Ordering Information

Table 2-4. Ordering information

Part number	Package	Operational temperature range
MT7615N	12*12*0.85 mm 118-DRQFN	TBD

2.7 TOP Marking Information

Figure 2-4. Top marking

3 Electrical Characteristics

3.1 Absolute Maximum Rating

Stresses beyond those conditions indicated in this section may cause permanent damage to the device.

Table 3-1. Absolute maximum ratings

Symbol	Parameters	Max. rating	Unit
AVDD33	3.3V supply voltage	-0.3 to 3.63	V
DVDD33	3.3V supply voltage	-0.3 to 3.63	V
AVDD16	1.68V supply voltage	-0.3 to 1.77	V
DVDD11	1.15V supply voltage	-0.3 to 1.265	V
T_{STG}	Storage temperature	-40 to +125	°C
VESD	ESD protection (HBM)	2000	V

3.2 Recommended Operating Range

Functional operation beyond those conditions indicated in this section is not recommended.

Table 3-2. Recommended operating range

Symbol	Rating	Min.	Typ.	Max.	Unit
AVDD33	3.3V supply voltage	2.97	3.3	3.63	V
DVDD33	3.3V supply voltage	2.97	3.3	3.63	V
AVDD16	1.68V supply voltage	1.6	1.68	1.77	V
DVDD11	1.15V supply voltage	TBD	1.15	TBD	V
$T_{AMBIENT}$	Ambient temperature	-10	-	70	°C

3.3 DC Characteristics

Table 3-3. DC description

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{IL}	Input low voltage	LVTTL	-0.28	0.6	V
V_{IH}	Input high voltage		2.0	3.63	V
V_{T-}	Schmitt trigger negative going threshold voltage	LVTTL	0.68	1.36	V
V_{T+}	Schmitt trigger positive going threshold voltage		1.36	1.7	V
V_{OL}	Output low voltage	$\|I_{OL}\|$ = 1.6~14 mA	-0.28	0.4	V

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{OH}	Output high voltage	$\|I_{OH}\|$ = 1.6~14 mA	2.4	VDD33+0.33	V
R_{PU}	Input pull-up resistance	PU=high, PD=low	40	190	KΩ
R_{PD}	Input pull-down resistance	PU=low, PD=high	40	190	KΩ

3.4 Thermal Characteristics

Table 3-4. Thermal information

Symbol	Description	Performance	
		Typ.	Unit
T_J	Max. junction temperature (plastic package)	125	°C
Θ_{JA}	Junction to ambient temperature thermal resistance[1]	15.73	°C/W
Θ_{JC}	Junction to case temperature thermal resistance	4.86	°C/W
Ψ_{Jt}	Junction to the package thermal resistance	1.11	°C/W

Note:
[1] JEDEC 4L 51-7 system FR4 PCB size: 76.2*114.3mm

3.5 Current Consumption

3.5.1 WLAN Current Consumption

Table 3-5. WLAN current consumption with integrated PA/LNA

Description	Performance	
	Typ.	Unit
Sleep mode	5	mA
2.4GHz RX Active, HT40, MCS31	350	mA
5GHz RX Active, VHT80, MCS9, Nss=4	710	mA
RX Power saving, DTIM=1	62	mA
RX Listen, BW80, Nss=4	355	mA
2.4GHz TX HT40, MCS31, @17.5dBm	1115	mA
2.4GHz TX HT40, MCS23, @17.5dBm	917	mA
5GHz TX VHT80, MCS9, Nss=4, @15dBm	1228	mA
5GHz TX VHT80, MCS0, Nss=4, @18.5dBm	1436	mA
2.4GHz TX CCK, 1Mbps @21.5dBm (2T)	870	mA

Note: TX power is measured at antenna port.

3.6 Wi-Fi RF Specification

3.6.1 Wi-Fi RF Block Diagram

The frond-end loss with diplexer:

- 2.4GHz insertion loss is 1.5 dB 1
- 5GHz insertion loss is 1.5 dB

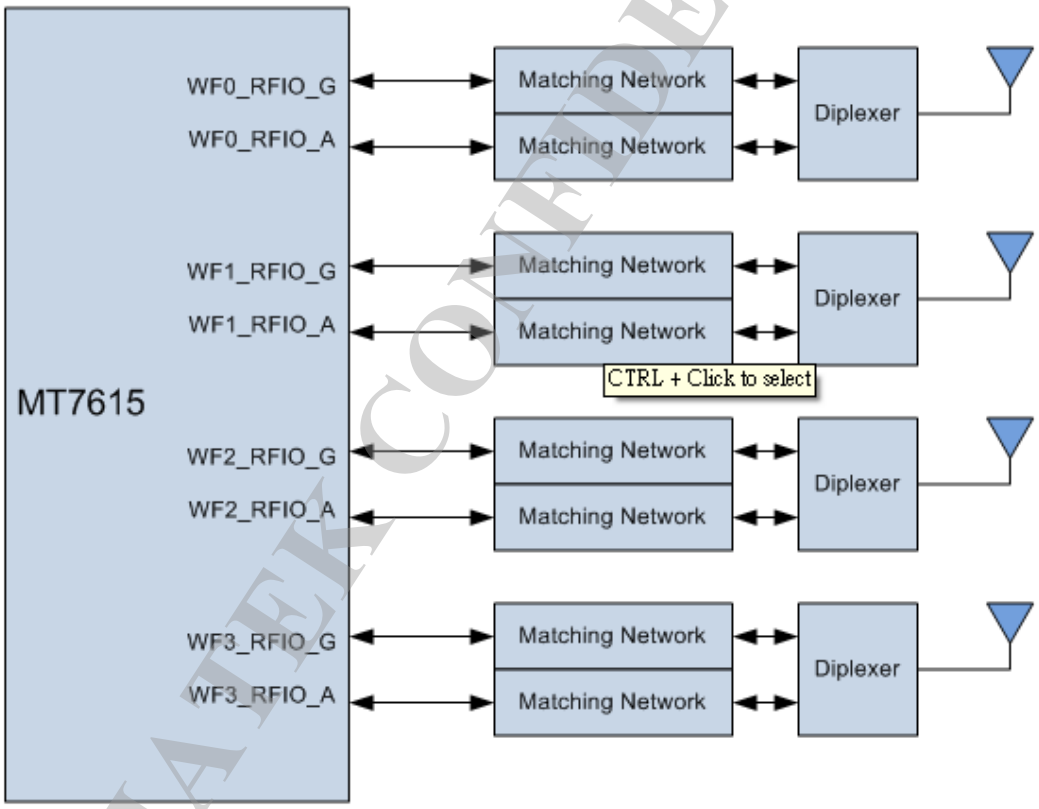


Figure 3-1 2.4/5GHz RF front-end configuration

3.6.2 Wi-Fi 2.4GHz Band RF Receiver Specifications

The specification in table below is defined at the antenna port, which includes the frond-end loss. (Assume FE loss=1.5dB)

Table 3-6. 2.4GHz RF receiver specifications

Parameter	Description	Performance			
		Min.	Typ.	Max.	Unit

Parameter	Description	Performance			
		Min.	Typ.	Max.	Unit
Frequency range		2412	-	2484	MHz
RX sensitivity	1 Mbps CCK	-	-97	-	dBm
	2 Mbps CCK	-	-94	-	dBm
	5 Mbps CCK	-	-92	-	dBm
	11 Mbps CCK	-	-89	-	dBm
RX sensitivity	6 Mbps OFDM	-	-94	-	dBm
	9 Mbps OFDM	-	-91.5	-	dBm
	12 Mbps OFDM	-	-91	-	dBm
	18 Mbps OFDM	-	-88.5	-	dBm
	24 Mbps OFDM	-	-85	-	dBm
	36 Mbps OFDM	-	-82	-	dBm
	48 Mbps OFDM	-	-77.5	-	dBm
	54 Mbps OFDM	-	-76.5	-	dBm
RX sensitivity BW=20MHz Mixed Mode 800ns Guard Interval Non-STBC	MCS 0	-	-93.5	-	dBm
	MCS 1	-	-90	-	dBm
	MCS 2	-	-87.5	-	dBm
	MCS 3	-	-84.5	-	dBm
	MCS 4	-	-81	-	dBm
	MCS 5	-	-77	-	dBm
	MCS 6	-	-75.5	-	dBm
	MCS 7	-	-74	-	dBm
	MCS 31	-	-73.5	-	dBm
RX sensitivity BW=40MHz Mixed Mode 800ns Guard Interval Non-STBC	MCS 0	-	-90	-	dBm
	MCS 1	-	-87	-	dBm
	MCS 2	-	-84.5	-	dBm
	MCS 3	-	-81.5	-	dBm
	MCS 4	-	-78	-	dBm
	MCS 5	-	-74	-	dBm
	MCS 6	-	-72.5	-	dBm
	MCS 7	-	-71	-	dBm
	MCS 31	-	-70.5	-	dBm
Maximum receive level	11 Mbps CCK	-	-5	-	dBm
	6 Mbps OFDM	-	-10	-	dBm
	54 Mbps OFDM	-	-10	-	dBm
	MCS0	-	-10	-	dBm
	MCS7	-	-10	-	dBm
Receive adjacent channel rejection	1 Mbps CCK	-	Note*	-	dB
	11 Mbps CCK	-	Note*	-	dB
	6 Mbps OFDM	-	Note*	-	dB
	54 Mbps OFDM	-	Note*	-	dB
Receive adjacent	MCS 0	-	Note*	-	dB

Parameter	Description	Performance			
		Min.	Typ.	Max.	Unit
channel rejection (HT20)	MCS 7	-	Note*	-	dB
Receive adjacent channel rejection (HT40)	MCS 0	-	Note*	-	dB
	MCS 7	-	Note*	-	dB

Note*: Receive adjacent channel rejection comply IEEE spec.

3.6.3 Wi-Fi 2.4GHz Band RF Transmitter Specifications

The specification in table below is defined at the antenna port, which includes the frond-end loss. (Assume FE loss=1.5dB)

Table 3-7. 2.4GHz RF transmitter specifications

Parameter	Description	Performance			
		Min.	Typ.	Max.	Unit
Frequency range		2412	-	2484	MHz
Output power	1~11 Mbps CCK	-	21.5	-	dBm
	6 Mbps OFDM	-	20.5	-	dBm
	54 Mbps OFDM	-	18.5	-	dBm
	HT40, MCS 0	-	19.5	-	dBm
	HT40, MCS 7	-	17.5	-	dBm
Output power variation[1]	TSSI closed-loop control across temperature and channels and VSWR ≦ 1.5:1.	-1.5	-	1.5	dB
Carrier suppression		-	-	-30	dBc
Harmonic output power	2nd Harmonic	-	-48	-	dBm/MHz
	3rd Harmonic	-	-48	-	dBm/MHz

Note 1: VDD33 voltage is within ±5% of typical value.

Note2: Second and third harmonic level correlate closely with diplexer's rejection (Please refer to HDK for diplexer p/n)

3.6.4 Wi-Fi 5GHz Band RF receiver specifications

The specification in table below is defined at the antenna port, which includes the frond-end loss. (Assume FE loss=1.5dB)

Table 3-8. 5GHz RF receiver specifications

Parameter	Description	Performance			
		Min.	Typ.	Max.	Unit
Frequency range		5180	-	5825	GHz
RX sensitivity	6 Mbps OFDM	-	-93	-	dBm

Parameter	Description	Performance			
		Min.	Typ.	Max.	Unit
	9 Mbps OFDM	-	-90.5	-	dBm
	12 Mbps OFDM	-	-90	-	dBm
	18 Mbps OFDM	-	-87.5	-	dBm
	24 Mbps OFDM	-	-84	-	dBm
	36 Mbps OFDM	-	-81	-	dBm
	48 Mbps OFDM	-	-76.5	-	dBm
	54 Mbps OFDM	-	-75	-	dBm
RX sensitivity BW=20MHz VHT Mixed Mode 800ns Guard Interval Non-STBC	MCS 0	-	-92.5	-	dBm
	MCS 1	-	-89	-	dBm
	MCS 2	-	-86.5	-	dBm
	MCS 3	-	-83.5	-	dBm
	MCS 4	-	-80	-	dBm
	MCS 5	-	-75.5	-	dBm
	MCS 6	-	-74.5	-	dBm
	MCS 7	-	-73	-	dBm
	MCS 8	-	-68.5	-	dBm
RX sensitivity BW=40MHz VHT Mixed Mode 800ns Guard Interval Non-STBC	MCS 0	-	-89	-	dBm
	MCS 1	-	-86	-	dBm
	MCS 2	-	-83.5	-	dBm
	MCS 3	-	-80	-	dBm
	MCS 4	-	-77	-	dBm
	MCS 5	-	-72.5	-	dBm
	MCS 6	-	-71.5	-	dBm
	MCS 7	-	-70	-	dBm
	MCS 8	-	-65.5	-	dBm
	MCS 9	-	-64	-	dBm
RX sensitivity BW=80MHz VHT Mixed Mode 800ns Guard Interval Non-STBC	MCS 0	-	-86	-	dBm
	MCS 1	-	-83	-	dBm
	MCS 2	-	-80	-	dBm
	MCS 3	-	-77	-	dBm
	MCS 4	-	-73.5	-	dBm
	MCS 5	-	-69.5	-	dBm
	MCS 6	-	-68	-	dBm
	MCS 7	-	-66.5	-	dBm
	MCS 8	-	-62.5	-	dBm
	MCS 9	-	-60.5	-	dBm
RX sensitivity BW=160MHz VHT Mixed Mode 800ns Guard Interval Non-STBC	MCS 0	-	-82.5	-	dBm
	MCS 1	-	-79.5	-	dBm
	MCS 2	-	-77	-	dBm
	MCS 3	-	-73.5	-	dBm
	MCS 4	-	-70.5	-	dBm

Parameter	Description	Performance			
		Min.	Typ.	Max.	Unit
	MCS 5	-	-66	-	dBm
	MCS 6	-	-64.5	-	dBm
	MCS 7	-	-63	-	dBm
	MCS 8	-	-59	-	dBm
	MCS 9	-	-56.5	-	dBm
Maximum receive level	6 Mbps OFDM	-	-10	-	dBm
	54 Mbps OFDM	-	-10	-	dBm
	MCS0	-	-10	-	dBm
	MCS7	-	-10	-	dBm
Receive adjacent channel rejection (VHT20)	MCS0	-	Note*	-	dB
	MCS8	-	Note*	-	dB
Receive adjacent channel rejection (VHT40)	MCS 0	-	Note*	-	dB
	MCS 7	-	Note*	-	dB
Receive adjacent channel rejection (VHT80)	MCS 0	-	Note*	-	dB
	MCS 7	-	Note*	-	dB

Note*: Receive adjacent channel rejection comply IEEE spec.

3.6.5 Wi-Fi 5GHz Band RF Transmitter Specifications

The specification in table below is defined at the antenna port, which includes the frond-end loss. (Assume FE loss=1.5dB)

Table 3-9. 5GHz RF transmitter specifications

Parameter	Description	Performance			
		Min.	Typ.	Max.	Unit
Frequency range		5180	-	5825	MHz
Output power	6 Mbps OFDM	-	19.5	-	dBm
	54 Mbps OFDM	-	17	-	dBm
	HT20, MCS 0	-	18.5	-	dBm
	HT20, MCS 7	-	16	-	dBm
	VHT80, MCS0	-	18.5	-	dBm
	VHT80, MCS9	-	15	-	dBm
Output power variation[1]	TSSI closed-loop control across temperature and channels and VSWR ≦1.5:1.	-1.5	-	1.5	dB
Carrier suppression		-	-	-35	dBc
Harmonic output rower	2nd Harmonic	-	TBD	-	dBm/MHz
	3rd Harmonic	-	TBD	-	dBm/MHz

Note 1: VDD33 voltage is within ±5% of typical value.

Note2: Second and third harmonic level correlate closely with diplexer's rejection (Please refer to HDK for diplexer p/n)

3.7 PMU Electrical Characteristics

Table 3-10. PMU electrical characteristics

Parameter	Conditions	Performance			
		Min.	Typ.	Max.	Unit
PCIE LDO					
Input voltage		1.51	1.68	1.84	V
Output voltage		1.14	1.2	1.26	V
Output current		-	-	40	mA
Quiescent current		-	60	-	uA

Note 1: The programmable range of the output voltage of the switching regulator is 0.8V to 2.3V.

4 Functional Specification

4.1 System

4.1.1 Power Management Unit

Power Management Unit (PMU) contains Two Low Drop-out Regulators (LDOs), power-on reset and the reference band-gap circuit. The circuits are optimized for quiescent current, drop-out voltage, and output noise.

Three power sources are required for MT7615, The 3.3V power source is directly supplied to EFuse LDO, digital I/Os, PCIe PHY, and RF related circuit. The 1.68V power source is supplied to PCIe LDO and RF related circuit. The 1.15V power source is supplied to digital circuit.

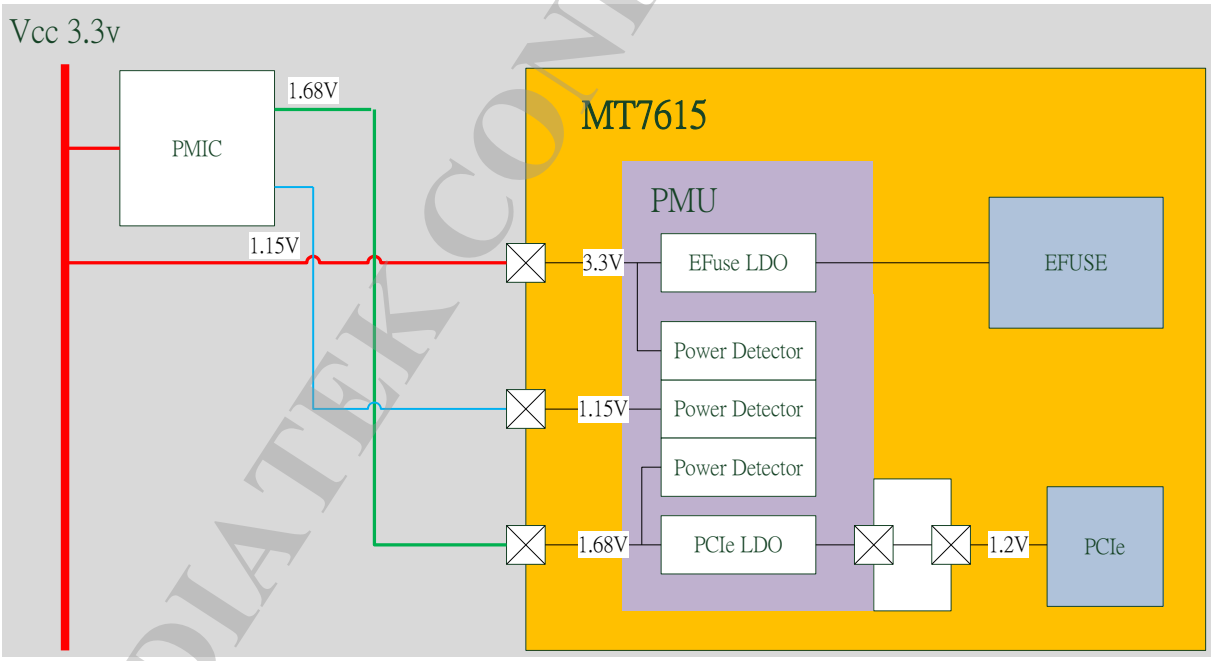


Figure 4-1. PMU block diagram

4.1.2 EFUSE

MT7615 uses embedded Efuse to store device specific configuration information such as MAC addresses, and power control settings.

Below illustrates the major fields defined in the Efuse.

- MAC addresses

- Wi-Fi configuration setting
- TSSI parameters, TX power level
- NIC configuration: RF front-end configuration, LED mode, baseband configuration
- Wi-Fi BeamForming parameter
- PCIe PHY parameters

It uses logical address mapping table scheme to make easy programming on efuse content.
The total efuse size is 7680 bits.

4.1.3 GPIO

MT7615 has 41 GPIO pins with software access. Pins are multiplexed with other functions including the LED control, external RF front-end module control, LTE coexistence, etc. Each GPIO supports internal pull-up/pull-down options as well as driving strength control.

4.2 Host Interface Architecture

4.2.1 PCI Express

MT7615 supports the high-speed interface which conforms to the PCI Express Base Specification v2.0. It supports PCIe link power states L0, L0s, L1, and L2. It also supports the new L1 sub-states to provide low power modes of operation.

The interface contains all necessary function blocks including transaction layer, data link layer, and physical layer. The standard configuration space and extended configuration space are supported.

4.3 MCU Subsystem

4.3.1 Network MCU Subsystem

MT7615 features ARM Cortex R4 processor.

R4 is a power efficient processor core with 8-stage dual issue pipeline and with tightly-coupled memory system. It is based on ARMv7R architecture with Thumb-2 / ARM instruction set.

It allows Wi-Fi functions to be performed on MT7615 and minimizes the computing power required for the host CPU.

4.3.2 Radio MCU Subsystem

MT7615 features Andes N9 processor and embedded ROM/RAM.

The radio MCU subsystem is used to perform Wi-Fi related functions. That includes the low power function that can minimize the loading of CR4 and the host CPU.

4.4 Wi-Fi Subsystem

4.4.1 Wi-Fi MAC

MT7615 MAC supports the following features:

- 802.11 to 802.3 header translation offload
- TCP/UDP/IP checksum offload
- Multiple concurrent clients as an access point
- Multiple concurrent clients as an repeater
- Aggregates MPDU RX (de-aggregation) and TX (aggregation)
- AMSDU in AMPDU support
- MU-MIMO supports four multi-user contains one primary user and three secondary users
- DBDC supports 2.4G/5G active concurrently
- Air time fairness and bandwidth control
- Transmit rate adaptation
- Transmit power control
- RTS with BW signaling
- CTS with BW signaling in response to RTS with BW signaling
- Security
  - 64-bit WEP (WEP-40) and 128-bit WEP (WEP-104) encryption with hardware TKIP processing
  - AES-CCMP and GCMP hardware processing
  - SMS4-WPI (WAPI) hardware processing

4.4.2 WLAN Baseband

MT7615 baseband supports the following features:

- Four spatial streams
- 11ac wave-1/2 feature
  - 5, 10, 20, 40, 80, 80+80, and 160MHz channels
  - MCS0-7 (BPSK, r=1/2 through 64QAM, r=5/6)
  - MCS8-9 (256QAM, r=3/4 and r=5/6)
  - VHT A-MPDU delimiter for RX and TX for single MPDU
  - Clear Channel Assessment (CCA) on secondary
  - Short Guard Interval
  - STBC
  - Low Density Parity check (LDPC) coding
  - SUBF
  - MU-MIMO (up to four users)
- Beamforming

  - Explicit Beamforming with support of NDP sounding
  - Explicit Beamforming with support of immediate feedback generation using compressed steering matrix
  - Proprietary Implicit Beamforming
- MU-MIMO configurations of
  - 4 users: 4*1ss
  - 3 users: 1*1ss + 1*2ss or 3*1ss
  - 2 users: 2*2ss or 1*1ss + 1*2ss or 2*1ss
- DBDC
- Digital pre-distortion to enhance PA performance
- Smoothing (channel estimation) extension to MIMO case
- Dynamic frequency selection (DFS) radar pulse detection
- Supports indoor location (802.11v)
- Proprietary dynamic channel bandwidth switching(DCBW) supports 160 2SS and 80 4SS packet-level transceiver concurrently.
- ProprietaryrReceiver MIMO power save scheme.

4.4.3 WLAN RF

MT7615 RF supports the following features:

- Integrated 4T4R 2.4GHz/5GHz PA and LNA
- Integrated 5GHz Balun
- 2.4GHz/5GHz external PA and LNA
- Improves the efficiency of RF PA with Digital Pre-Distortion (DPD)
- Improves the power variation with TSSI compensated TX power control

ESD CAUTION

MT7615 is ESD (electrostatic discharge) sensitive device and may be damaged with ESD or spike voltage. Although MT7615 is with built-in ESD protection circuitry, please handle with care to avoid the permanent malfunction or the performance degradation.